DIGITAL SELF-TUNING TECHNIQUE FOR CONTINUOUS-TIME FILTERS

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ABSTRACT

In this paper a new auto-tuning digital technique is reported for continuous-time filters over VHF applications, based on phase detector. By using a 0.35 µm digital CMOS process, changes in frequency response of a 3thr-order low pass filter can be tuned with a 3.1% error over the designed value. This technique confirms the feasibility of the proposed scheme in continuous–time filter applications. The system consumes less area, power and tuning time than other proposed schemes. Simulated results show the building viability in a 10 MHz low pass filter.

1. INTRODUCTION

The continuous-time technique has been used to implement filters where high frequency at low cost of silicon and power is required, instead of the switched-capacitor or switched-current approaches [1]-[3]. The low cost CMOS technology is a good choice if the requirement of accuracy is relaxed and is the most economical solution if the whole system is implemented in a pure digital process. Among high speed processing signal applications, it is widely used in the IF band pass sections of RF front-end circuits and in the hard disk drive industry. These applications demand continuous-time filters with variable bandwidths over a wide range [4]. A possible solution could be to use discrete tuning for IF filters, in the same way that this technique is being used in other high frequency applications, such as IF-baseband strips [5] or read-channel filters [6].

On the other hand, we must not overlook the problems encountered on the analogue part in the current digital CMOS processes associated with the scaling down and low-voltage operation. Among these, the reduced dynamic range is of concern, making difficult conventional continuous tuning, used to compensate technological and temperature spreads, which degrades the dynamic range. So, it is necessary to provide an on-chip automatic tuning scheme to achieve an accurate filter performance [7]-[8]. This circuit tunes the characteristic filter frequency in order to compensate fabrication tolerances, temperature variations and ageing. We can take advantage of the simplicity of the digital control algorithms to adjust the tuneable analogue part by the digital algorithm thus yielding a considerable saving of area and power.

In this paper, an innovative frequency digital auto-tuning algorithm is presented for use in integrated continuous-time filters which is simpler than other schemes [9]-[10] and which needs less silicon and power. 4-bit digitally auto-tuned third order low-pass filter was simulated using this technique yielding a 10 MHz fixed cut-off frequency low-pass filter with an error below 3% and tuning time lower than 1.6 µs. Simulation results and Monte Carlo analysis show the implementation viability and are presented in this communication.

In section 2, a description of the overall system and its basic component blocks description are presented. Section 3 presents the proposed phase detector deep viability study with simulation results and Monte Carlo analysis. Conclusions are given in section 4.

2. SYSTEM DESCRIPTION

2.1. Auto-Tuning Scheme

The whole system is made up of four blocks: an analogue filter with digitally tuneable characteristic frequency, a delayer stage, a phase detector and an up/down counter. The global system arrangement is depicted in Figure 1.

A high accuracy reference harmonic signal V_{ref} at desired filter characteristic frequency is fed into the system. This signal goes through the digitally tuneable analogue filter, yielding signal A, and into the delayer block, yielding signal B. At filter output, the signal suffers a known delay which depends on the filter type and its characteristic frequency. The delayer block must provide the same delay as the filter caused by the filter over the reference signal when working at the desired characteristic filter

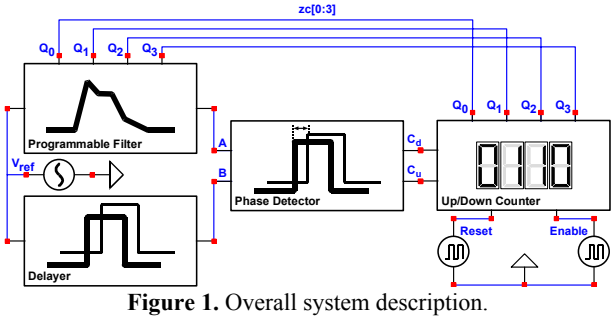

Figure 1. Overall system description.

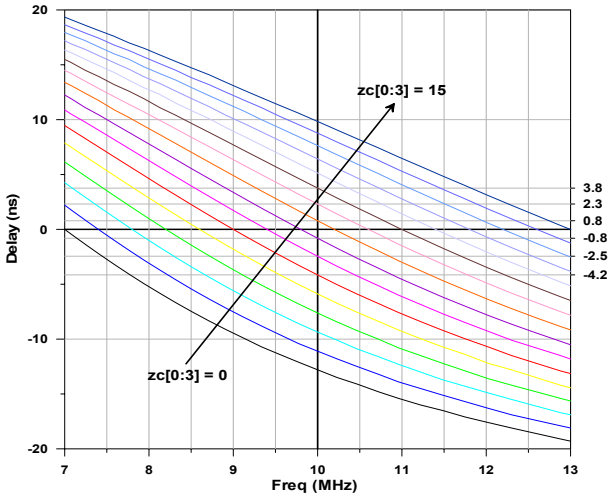

Figure 2. AHDL-described tunable filter delay response.

frequency. Only when the filter is not working at the desired characteristic frequency is there a lag between the filter and delayer outputs (A and B). The filter and delayer outputs are led into the phase detector in order to compare their relative phases. This block generates one pulse per cycle in the C_d (down) output, if the filter output signal goes ahead, and one pulse per cycle in the C_u (up) output when the filter signal is delayed. In this way, C_u and C_d signals control the up/down counter, the state of which is used to control the digitally tuneable analogue filter. When parameters such as programmability range, phase detector resolution and up/down counter bits are properly selected, the system stabilizes at the state with the filter tuneable characteristic frequency closest to the reference signal frequency.

The 4-bit digitally tuneable characteristic frequency filter was described using AHDL and reproduces the behaviour of a third order low pass filter. Figure 2 shows the delay with regard to the lag caused by the filter working at the desired characteristic frequency, for each zc[0:3] value. As can be observed, the filter characteristic frequency can be linearly adjusted from 7 MHz to 13 MHz using the controlling 4-bit digital word. A 10 MHz characteristic frequency filter was selected in order to prove the technique viability.

The delayer block can be implemented in several ways depending on the filter phase response. To show the proposed system functionality a VERILOGA-described delayer cell was used in this work.

A standard up/down binary counter with reset, enable and

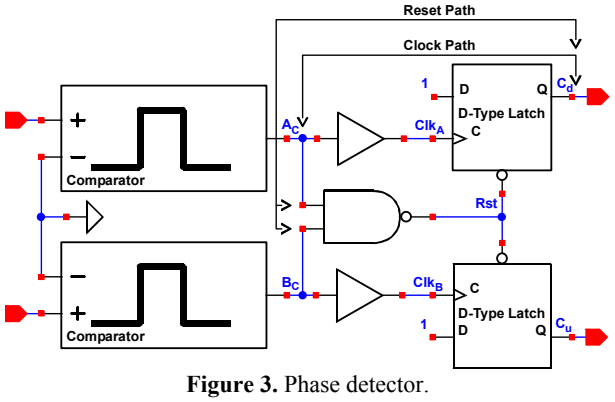

Figure 3. Phase detector.

separate up/down clocks was used with minimal changes; a control which prevents 0 to 2^n-1 and 2^n-1 to 0 transitions was implemented. On the other hand, the more significant bit was stored in T flip-flops with reset control, while the rest of the bits where stored using T flip-flops with set control. In this way the system starts to count from 2^{n-1}-1=7 (that is, starting cut-off frequency at 9.8 MHz) after a reset signal instead of starting from 0 or 2^{n-1}.

2.2. Phase Detector Block

The signals to be compared, A and B, are driven through VERILOGA-described identical comparators to provide digital square shape signals to the next stages, A_C and B_C as shown in Figure 3.

These two conditioned signals are connected to the clock inputs of identical D-type flip-flops through a buffer. At the same time each of the conditioned signals is connected to each one of a NAND gate input whose output is attached to both of the flip-flop reset inputs (see Figure 3). The flip-flop D inputs are fixed to 1. This topology ensures that only one or none of the flip-flops loads the D input per cycle, if the Rst signal arrives faster than the Clk_A and Clk_B signals to the flip-flops; that means the "Clock Path Delay" has to be shorter than the "Reset Path Delay" (CPD and RPD respectively in Figure 4). These path delays ensure that the reset signal resets the flip-flips faster than the clock signal changes the flip-flop state. These delays also set the resolution of the system matching the filter output signal phase with the delayer output signal phase as can be seen in the next section. This issue makes the phase detector the most delicate block as it requires precise clock path delay stages between A_C and B_C and flip-flop clocks and resets.

2.3. Phase Detector Operation Principle

The phase detector must provide a pulse per cycle in C_d and no change in C_u if A is ahead, and if B is ahead, a pulse per cycle in C_u and no pulse in C_d. To prevent undesired pulses, A_C to C_d delay (CPD) and B_C to C_u

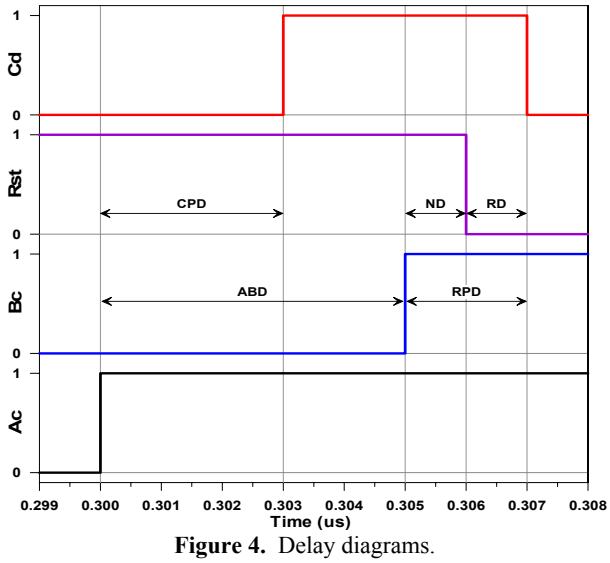

Figure 4. Delay diagrams.

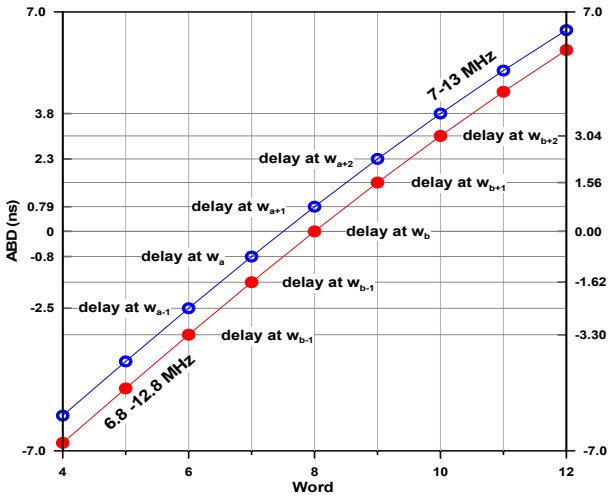

Figure 5. ABD for every digital word for two different AHDL described filters centred at 10 MHz and 9.8 MHz.

delay (same delay) must be longer than the delay via reset (B_C to C_d/C_u if A_C arrives first at the NAND gate). Furthermore, the system must not discriminate A to B lags shorter than a certain quantity if we want the system to stabilize at the best possible digital word.

Imagine A is ahead of B and let's call this lag ABD (see Figure 4). The A_C rise forces the flip-flop to load D value, which is fixed at 1, after CPD. This produces a rise in the C_d signal and the up/down counter counts down 1 (see Figure 3 and 4). When the B_C rise occurs, it changes the NAND gate state causing activation of the flip-flop reset and the C_d signal to drop after ND + RD. The pulse width generated in C_d is equal to ABD – CPD + (ND + RD). The latter parenthesis is the "Reset Path Delay", RPD as can be seen in Figure 3 and 4. When ABD < CPD – RPD there is no pulse in C_d. As the lag from the B_c rise up to C_u rise is CPD too, the C_u state does not change and there is no pulse in C_d nor C_u.

The phase Detector operation principle is based on achieves an accurate delay difference between the CPD lag and RPD lag. Because of the symmetry of the system with regard to the A_C and B_C signals the same occurs if B_C is ahead.

2.4. Timing Calculation

As shown in section 2.3, a pulse is generated if the lag between A and B (ABD) is bigger than CPD – RPD; we shall name this latter quantity "relative delay between clock path and reset path": RDCR. The phase detector does not react for shorter values of ABD than RDCR, this quantity fixes system accuracy matching tuned characteristic frequency with desired characteristic frequency. This lag must be calculated according to the desired characteristic frequency, tuning bit number and characteristic frequency filter integration accuracy.

Two timing restrictions must be achieved. Firstly, the system must reach the best possible digital word and secondly it must stabilize at this word without generating any pulse at either the C_u or the C_d outputs.

To achieve the first aim, the phase detector must perceive any delay longer than the ABD at this digital word. The more restrictive case is when the desired frequency matches a digital word exactly, like w_b in Figure 5 (where the representation of ABD versus the tuning digital word are depicted for tow AHDL described filters). In this situation RDCR must be shorter than the shortest between at w_{b-1} and at w_{b+1} delay. In Figure 5 this condition is satisfied if RDCR < 1.56 ns. On the other hand, the system must stabilize at the desired state, to ensure this situation the phase detector has not to notice delays shorter than the delay achieved at this state. In this case the worst situation is when the desired frequency matches exactly in the middle between two consecutive digital words, w_a and w_{a+1}, as depicted in Figure 5. RDCR must be longer than the longest ABD at these digital words. From Figure 5 we see this is satisfied if RDCR > 0.8 ns. We can see the phase detector has not to generate any output pulse if ABD is shorter than 0.79 ns and must generate a pulse if the lag is greater than 1.59 ns, in this case RDCR must satisfy: 0.79 ns < RDCR < 1.56 ns to ensure that the system stabilizes at the best digital word.

3. PHASE DETECTOR VIABILITY STUDY: SIMULATION RESULTS

As shows in Section II, the phase detector requires precise relative delay path implementation between reset and clock paths, RDCR (see Figure 3). Theoretically, this lag has to be fixed between 0.8 ns and 1.5 ns. Evidently, the best choice is 1.2 ns but this lag could change due to mismatching, ageing, temperature changes and working conditions. To ensure the viability of the system several simulations were carried out. In Figure 3 each element was substituted by AMS c35b3 process library elements. For each element type, the smaller was used. The buffers were changed for 7 library buffers (BUF2) in serial arrangement, this configuration provides a clock path delay (CPD) of approximately 1.35 ns using library flip-flops (DFC1). The NAND gate was NAND20 and provides a reset path delay (RPD) of 0.36 ns. Simulation results show this arrangement can detect delays between

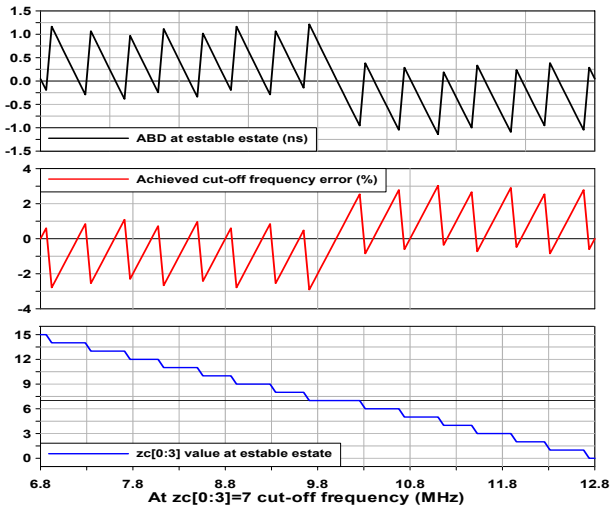

Figure 6. Final ABD, cut-off frequency error and zc[0:3] value after tuning process versus AHDL-described filter at zc[0:3]=7 cut-off frequency.

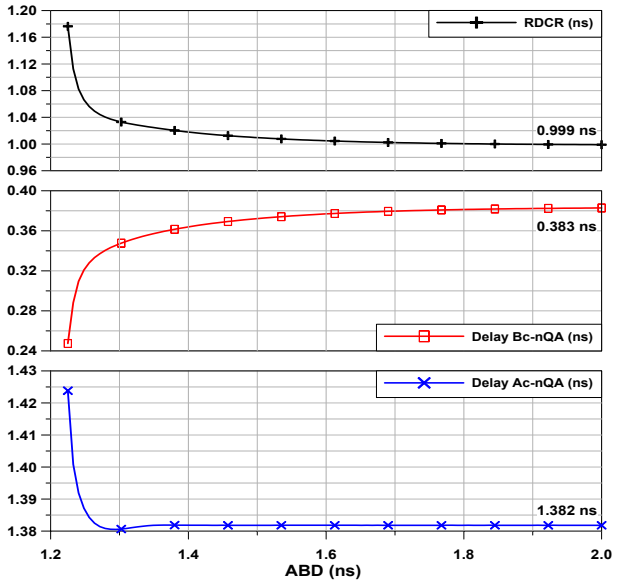

Figure 7. Delay study versus ABD lag.

A_c and B_c (ABD) longer than 1.225 ns.

Due to the building process, ageing and temperature changes, tuneable filter starting cut-off frequency (frequency at zc[0:3] = 7) can be from 6.86 MHz to 12.74 MHz (if it is designed to be 9.8 MHz and considering the mentioned 30% error). Figure 6 represents tuneable filter parameters after the tuning process for 100 AHDL-described tuneable filters with, at zc[0:3]=7 from 6.8 MHz to 12.8 MHz, represented in the x-axis. As can be seen the error is lower than 3.1 %. The maximum tuning time was only 1.6 µs.

In Figure 7 RPD, CPD and RDCR dependences with ABD are presented. As can be seen, this dependence is appreciable only when the relative (A_c, B_c) lag is shorter than 1.3 ns. At working frequencies this issue does not limit the tuning range (at any ABD value, RDCR < 1.20 ns) but to reach higher characteristic frequency filters, the implementation must be done using faster technologies with a shorter channel length.

Figure 8 depicts phase detector Monte Carlo analysis results. This analysis was carried out without correlation definition for any element. Analysis results predict a RDCR compatible with the calculated values, this means the building process will not significantly affect the phase detector resolution if a careful layout is developed.

4. CONCLUSIONS

A new auto-tuning methodology is presented in this paper. Working principle is based on a phase detector with accurate relative path delays implementation. Preliminary studies show the phase detector building viability. The tuning scheme was simulated on an AHDL code for a Butterworth third-order low-pass filter yielding a 10 MHz cut-off frequency filter with an error lower than 3.1 % and a tuning time of 1.6µs.

5. REFERENCES

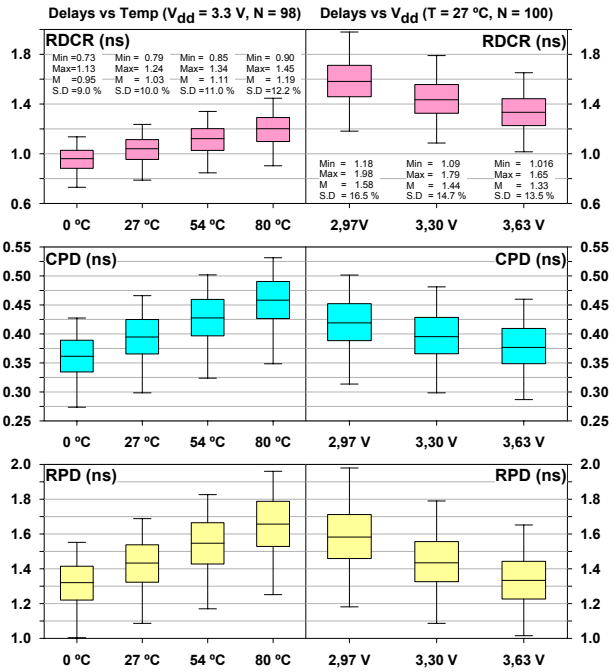

Figure 8. Critical phase detector delays box and whisker plots versus temperature and bias voltage (V_{dd}). ABD = 2ns.

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